forming a second metal oxide semiconductor radio frequency circuit element over a second triple well in a substrate; and

A2 cont.

biasing a second well of said second triple well through a second resistor coupled to said first bias potential.

Please cancel claim 25.

Please amend claim 26 as follows:

A3

26. (Amended) The method of claim 20 including biasing said wells through resistors having a resistance greater than 100 ohms.

Please add the following new claims 30 *et seq.*:

31. (New) A method comprising:

forming a metal oxide semiconductor circuit element over a triple well in a substrate;

operating said circuit element at a radio frequency; and

biasing a well of said triple well through a resistor which acts as a high impedance relative to a junction capacitance within the triple well.

A4

32. (New) The method of claim 31 including forming an integrated inductor over said triple well.

33. (New) The method of claim 31 including forming a P-type well in an N-well formed in said substrate.

34. (New) The method of claim 33 including biasing the N-type and P-type wells through different resistors.

35. (New) A method of claim 31 including providing a common bias potential to different wells through separate resistors for each well.

36. (New) The method of claim 35 including biasing said wells through resistors having a resistance greater than 100 ohms.

37. (New) The method of claim 31 including coupling a resistor to an N-well within said triple well on a P-type substrate so that said resistor acts as a high impedance relative to the junction capacitance of the N-well to the P-well of the triple well.

A4 Cont.

REMARKS

When the resistor bias is utilized in an environment wherein a MOS circuit element is positioned over the triple well and that element operates in the radio frequency range, the AC characteristics of the circuit are improved. Namely, when a resistor is coupled from supply to an N-well inside a triple well on a P-type substrate, for RF frequencies, the resistors act as a high impedance relative to the junction capacitance of the N-well to P-well inside the N-well. Then for a MOSFET inside the P-well will see less loading through this well junction capacitance in series with the resistor. A similar point can be made where the resistor is coupled to the P-well.

Thus, it is the AC characteristics of the circuit that are improved and it is not just the simple biasing through a resistor. As amended, the claims make this distinguishing point.

Nothing in any of the references cited in any way suggest the advantages that can be achieved at radio frequencies using resistor bias. Therefore the invention should patentably distinguish over all of these references.

As explained on page 27 of the present application, use of the triple well applied to the common gate transistor 314 of the cascode circuit 310 reduces the output 10 capacitance to achieve higher output bandwidth. It is explained at the bottom of page 29 and the top of page 30 that noise coupling is more acute in connection with radio frequency devices and that radio frequency devices are devices that operate at frequencies above 1 MegaHertz.

Furthermore, it is noted in the specification that the word triple well does not encompass a bipolar transistor. The cited *Ryerson* reference is a bipolar transistor and thus is not of any pertinency.